second and third sections added together or the impedance of each one separately. From the context of the specification, it is clear that the impedances are of each of the second and third sections separately. (See, for example, page 13, line 19 – page 14, line 7.) However, to make explicit what was already implicit, claims 1 and 12 are amended to add the word "each" following the phrase "impedances of the second and third sections."

3. The Office action requests clarification as to what is intended by the impedances of the first section. The impedances of the first section are the impedances of the conductors of the first section. Impedances are measured in ohms. (See, for example, page 13, line 19 – page 14, line 7.)

35 U.S.C. § 103(a) rejections. Claims 1-23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Prior art figure 1a of Fan et al. (Patent 6,381,164) in view of Fan et al. figure 2a.

Independent claims 1, 11, and 16 each recite: "a path including conductors in a first section that splits into a second section and third section ...."

In contrast to the claims, neither figure 1a nor figure 2a of Fan et al. show a first section of a path of conductors splitting into a second and third section. Accordingly, the rejections should be withdrawn.

Note that there are other patentable distinctions between the claims and Fan et al.

Applicant believes the application is in condition for allowance and respectfully requests the same.

Respectfully submitted,

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APPENDIX:

Please amend the application as follows:

MARKED UP VERSION OF THE CLAIMS

1. (Amended) A system comprising:

first and second modules, the first module having a first group of chips and the second module having a second group of chips;

a circuit board including first and second module connectors to receive the first and second modules, respectively;

a first buffer on the first module and a second buffer on the second module; and

a path including conductors in a first section that splits into a second section and third section, wherein the second section couples to the first buffer and the third section couples to the second buffer, and wherein the first buffer provides signals received from the second section to the first group of chips and the second buffer provides signals received from the third section to the second group of chips, and wherein impedances of the second and third sections are each at least 50% greater than impedances of the first section.

12. (Amended) The system of claim 11, wherein impedances of the second and third sections are each at least 50% greater than impedances of the first section.